EIA/JESD51-3

EIA/JEDEC STANDARD

Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

EIA/JESD51-3

AUGUST 1996

ELECTRONIC INDUSTRIES ASSOCIATION

ENGINEERING DEPARTMENT

Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(From JEDEC Council Ballot JCB-95-40, formulated under the cognizance of JC-15.1 Committee on Thermal Characterization Techniques for Electronic Packages and Interconnects.)

1 Background

1.1 The measurement of the Junction-to-Ambient (θ_{JA}) thermal characteristics of an integrated circuit (IC) package has historically been carried out using a number of test fixturing methods. The most prominent fixturing method is the soldering of the packaged devices to a printed circuit board (PCB). The characteristics of the test PCB's can have a dramatic (>60%) impact on the measured θ_{JA}. Due to this wide variability, it is desirable to have an industry wide standard for the design of PCB test boards to minimize discrepancies in measured values between companies.

1.2 To obtain consistent measurements of θ_{JA} from one company to the next, the test PCB geometry and trace layout must be completely specified for each package geometry tested. Such a complete specification would limit the flexibility of user companies who would like to design test boards for their individual needs. Thus, one characteristic of a test board specification is to allow some variability of PCB test board design while minimizing measurement variability.

1.3 This specification should be used in conjunction with the electrical test procedures described in JEDEC Standard No. 51-1, "Integrated Circuit Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device)," [1], and JEDEC Standard No. 51-2, "Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air)," [2].

1.4 References

[1] JEDEC Standard No. 51-1, "Integrated Circuit Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device)."

[2] JEDEC Standard No. 51-2, "Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air)."

[3] Surface Mount Land Patterns (Configurations and Design Rules), Pub. No. ANSI/IPC-SM-782 (782A), Developed by the Institute for Interconnecting and Packaging Electronic Circuits, 1987.

[4] "Electronics Engineer's Handbook," 3rd Edition, Edited by D.G. Fink and D. Christiansen, McGraw-Hill Book Co., NY, 1989, p 6.16

[5] MIL standard MIL-W-5088B

2 Scope

2.1 This specification covers leaded surface mount components of lead pitch greater than 0.35 mm up to a body size of 48 mm. It is not intended for through-hole, ball grid array, or socketed components. See the appropriate test specifications for these package types.

3 Purpose

3.1 The purpose of this proposal is to describe parameterized guidelines for thermal test board design with a "low" effective thermal conductivity (1 signal layer in the trace fan-out area) compared to a multi-layer PCB which might include power and ground planes. The resulting test PCB's will show less than 10% PCB related variation in measured θ_{JA} for a given package geometry within the maximum and minimum range of all variable parameters. The specified parameters impact the area of the test board, the amount of copper traces (Cu) on the test board, and the resulting trace fan-out area, all important parameters to the heat sinking characteristics of the PCB. It should be emphasized that values measured with these test boards cannot be used to directly predict any particular system application performance but are for the purposes of comparison between packages.

4 Stock material

4.1 The test PCB shall be made of FR-4 material. The material shall be 1.57 mm (0.062") +/- 10% thick. For high temperature applications, > 125°C, use of other test board material is acceptable as long as the thermal conductivity of the material is reported and measurement correlations have been established between the substitute material and FR-4.

5 Board outline

5.1 The board shall be 76.2 mm x 114.3 mm (3.0" x 4.5") +/- 0.25 mm (0.010") in size for packages less than 27.0 mm (1.06") on a side as shown in figure 1; or 101.6 mm x 114.3 mm (4.0" x 4.5") +/- 0.25 mm (0.010") in size for packages with a maximum body length from 27.0 mm (1.06") to 48.0 mm (1.9") as shown in figure 2. A typical edge connector is depicted in figure 1. The edge connector can be pin-out and pitch modified for company specific needs. Width modification of dimension F is allowed. Multiple rows of vias along the edge connector are allowed.

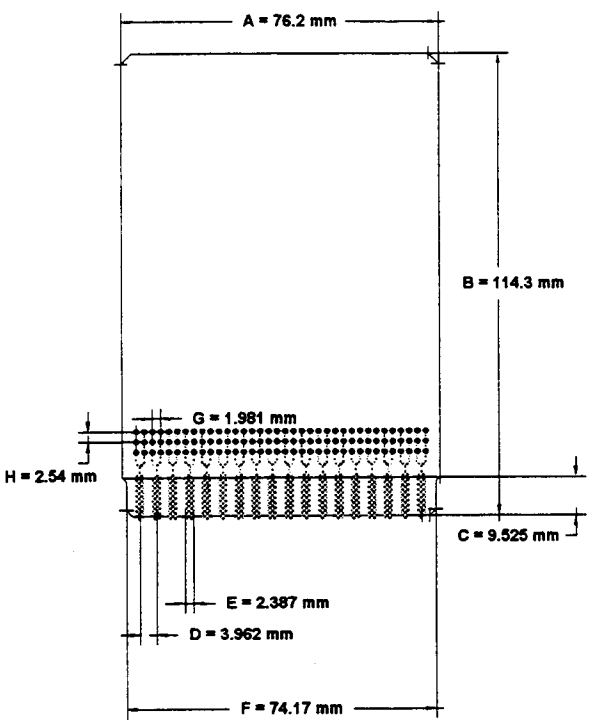

Figure 1: PCB for packages <27 mm

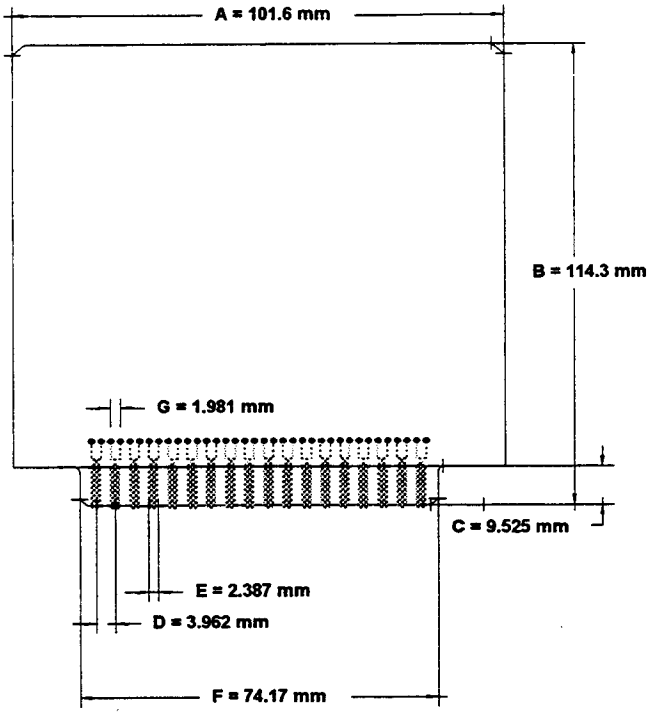

Figure 2: PCB for package ≥27 mm

6 Trace design:

6.1 Trace Layout: Traces should be laid out such that the test device will be centered relative to a 76.2 mm x 76.2 mm (3.0" x 3.0") square in the section of the test board furthest removed from the edge connector for packages <27 mm and centered in a 101.6 mm x 101.6 mm (4.0" x 4.0") section for packages ≥27 mm. The traces connecting to the package must extend at least 25 mm out from the edge of the device body. Trace lengths longer than this amount are allowed. For 4 sided packages, traces must be flared to meet the edges of a square such that the terminal via locations are equally spaced over 90% of the perimeter of the sides of this square adjacent to the leaded sides of the package (figure 3). For packages with leads on 2 sides, traces may be flared or straight to meet plated through holes on 2.54 mm (0.1") centers (figure 4). For 4-sided designs, staggering of trace terminal soldering positions inward from the trace termination square is allowed to 2.54 mm (0.1") off the perimeter of the square (figure 5). For inline packages (2 sided designs), the length axis of the package must align with the length axis of the test PCB. For 2-sided designs, staggering of trace terminal soldering positions 2.54 mm (0.1") inward from the 25 mm minimum trace length is allowed only when the number of pins per side multiplied by 2.54 mm is greater than 75 mm for the smaller PCB and greater than 100 mm for the larger PCB. A trace design that nests packages with equal pin pitches on the same PCB is allowed as long as the above conditions are met (figure 5).

6.2 Trace Widths: Trace widths shall be 0.254 mm (0.010") wide +/-10% at finish size for 0.5 mm or larger pin pitches. For finer pin pitches, the trace width shall be set to the lead width. Achieving the finish size may require some oversize in design to compensate for over-etching of the Cu traces during processing. Traces should terminate in a plated through-hole for soldering interconnect purposes. See 6.8 for a description of the plated through-hole vias. Solder land patterns should conform to the package lead outlines as described in ANSI/IPC publications [3]. No solder lands should be designed in the nested configuration; instead, the traces in thesoldering region to the outer most lead tip of the largest package should be the same width as the lead before immediately necking down to 0.254 mm (0.010").

6.3 Trace Layers: The package fan-out trace layer will consist of traces on the top of the PCB only; bottom layer traces are not allowed within the fan-out region.

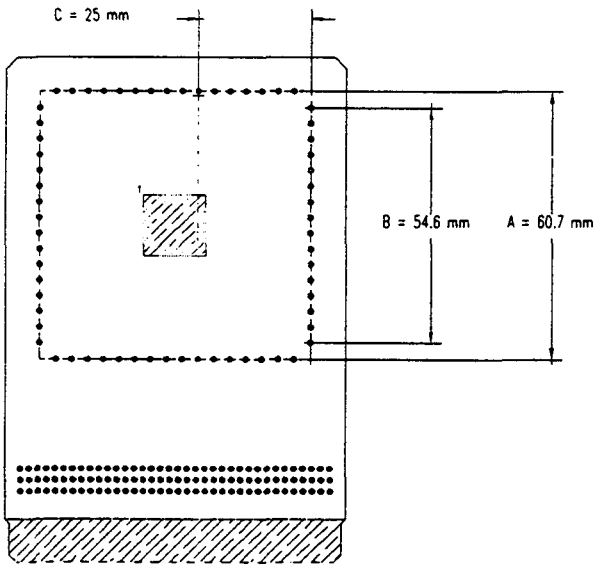

Figure 3: Traces flared to square @ 25 mm from package body

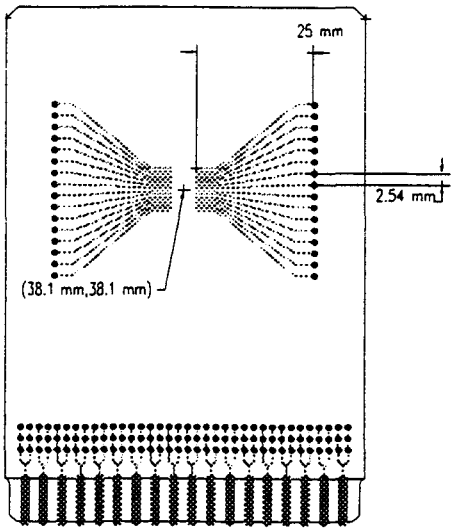

Figure 4: Traces flared to 2.54 mm centered vias @ 25 mm from package body

6.4 Connection Routing: Trace connection to the edge connector using either the top or bottom trace layers is allowed if the interconnection remains outside the flared perimeter (fan-out area) of the through holes (figure 6). No traces are allowed to run under the PCB inside the flared perimeter of the through holes. Measurement force (power) and sense (measure) lines should be independent of each other when routed from the edge connector to the package pins.

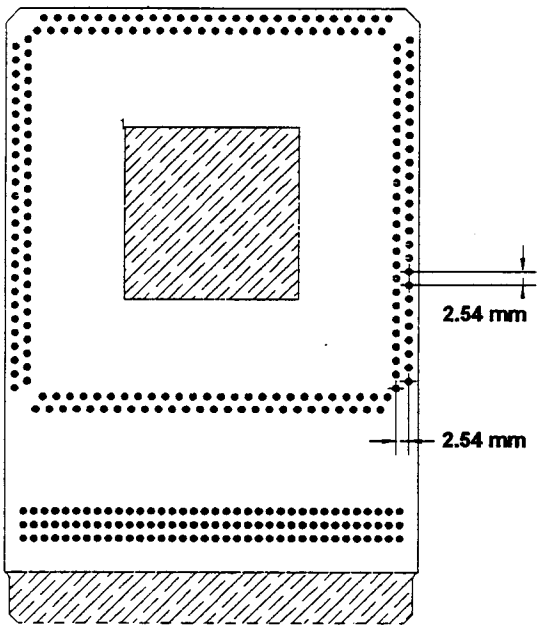

Figure 5: Nested PCB design (44-176PQFP) outside

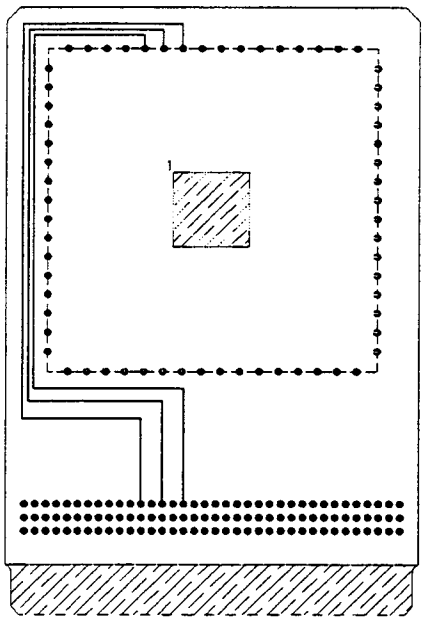

Figure 6: Connection routing fan-out perimeter (optional)

6.5 Wiring to the Edge Connector: Manual wiring from the through holes to the edge connector shall be made with 22AWG copper wire (0.64 mm; 0.0254" diameter) or smaller if the connections are not designed as part of the trace pattern. Interconnect wiring to the edge connector shall be on the trailing edge of the board with respect to air flow direction and back side of the board with respect to the component placement. Interconnect wiring shall be outside the fan-out area. Connection from the edge connector to the fan-out perimeter and from the fan-out perimeter to the power dissipation structures must be made in a four point method for force (power) and sense (measure) purposes. Wire and through hole diameters for heater force currents may need to be larger to accommodate high power tests. Use table 1 as a guide to determine the required wire diameter [4,5].

Table 1 — Wire Size Current Limits

AWG Wire Size	UL Current Capacity, (80 °C), Amperes	MIL-W-5088B Amperes
30	0.4	na
28	0.6	na
26	1.0	na
24	1.6	na
22	2.5	5.0
20	4.0	8.33
18	na	15.4
16	na	19.4
14	na	31.2
12	na	40

6.6 PCB Metalization Characteristics: Metalization on the PCB should be 2 oz finished thickness after final processing (0.071 mm; 0.0028"). This is achieved by starting with a 1 oz Cu material and plating to 2 oz during PCB through hole plating process. This process specification should be printed on all drawings to insure proper processing. The thickness of the Cu tracks should be verified to +/- 20% after PCB fabrication since thickness variations greater than this can have an influence on the performance of the PCB.

6.7 Solder Masks: Solder masking is optional.

6.8 Plated Through Hole Vias: The plated through hole vias should have a solder land diameter of no less than 1.27 mm (0.05") with a drill hole of no less than 0.83 mm (0.033").

7 Data presentation

7.1 Table 2 lists parameters specified by this document. The "user" column allows the user to input actual measured values from his test boards.

Table 2 — Specified parameters and values used

Dimension	Specification	Used
Board Thickness	1.57 mm (0.062")	
Board Dimension (pkg length< 27 mm)	76.2x114.3 mm (3.0"x4.5")	
Board Dimension (27 mm £ pkg length £ 48 mm)	101.6x114.3 mm (4.0"x4.5")	
Board Material	FR-4	
Fan-out Trace Length (minimum)	25 mm (0.98")	
Fan-out Trace Position	centered in 76.2x76.2 mm or 101.6x101.6 mm section	
Trace Thickness	0.071 mm (0.0028") +/-20%	
Trace Width in Fan-out Region	0.254 mm (0.01") +/-10% for ³ 0.5 mm pin pitch; Lead width for < 0.5 mm pin pitch	
Trace Width in Nested Lands	Lead width	
Trace Coverage Area (total)		
Nested/Not Nested	yes/no: package body sizes nested	
Solder Mask	yes/no: type	
Via Spacing	2.54 mm (0.1")	
Via Land	1.27 mm (0.05")	
Via Drill Hole	0.83 mm (0.033")	
Wire Gauge (Sense)	22AWG (0.64 mm; 0.0254" diameter)	
Wire Gauge (Heater Force)		